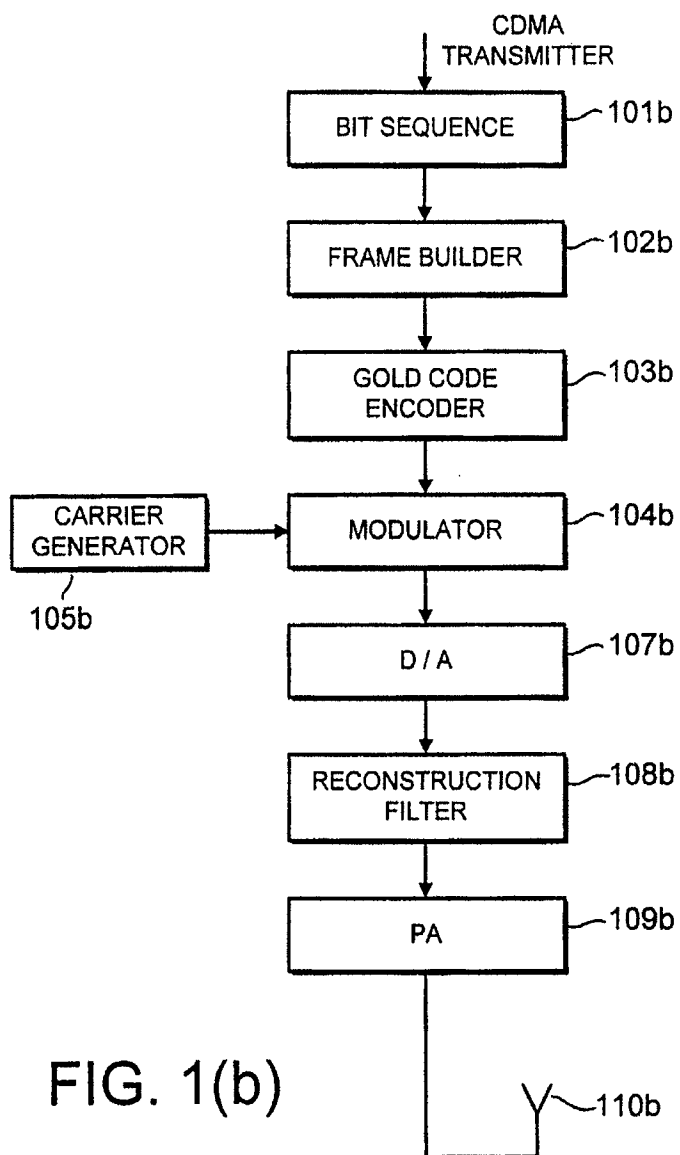


FIG. 1(a)

PRIOR ART

**FIG. 1(b)**

PRIOR ART

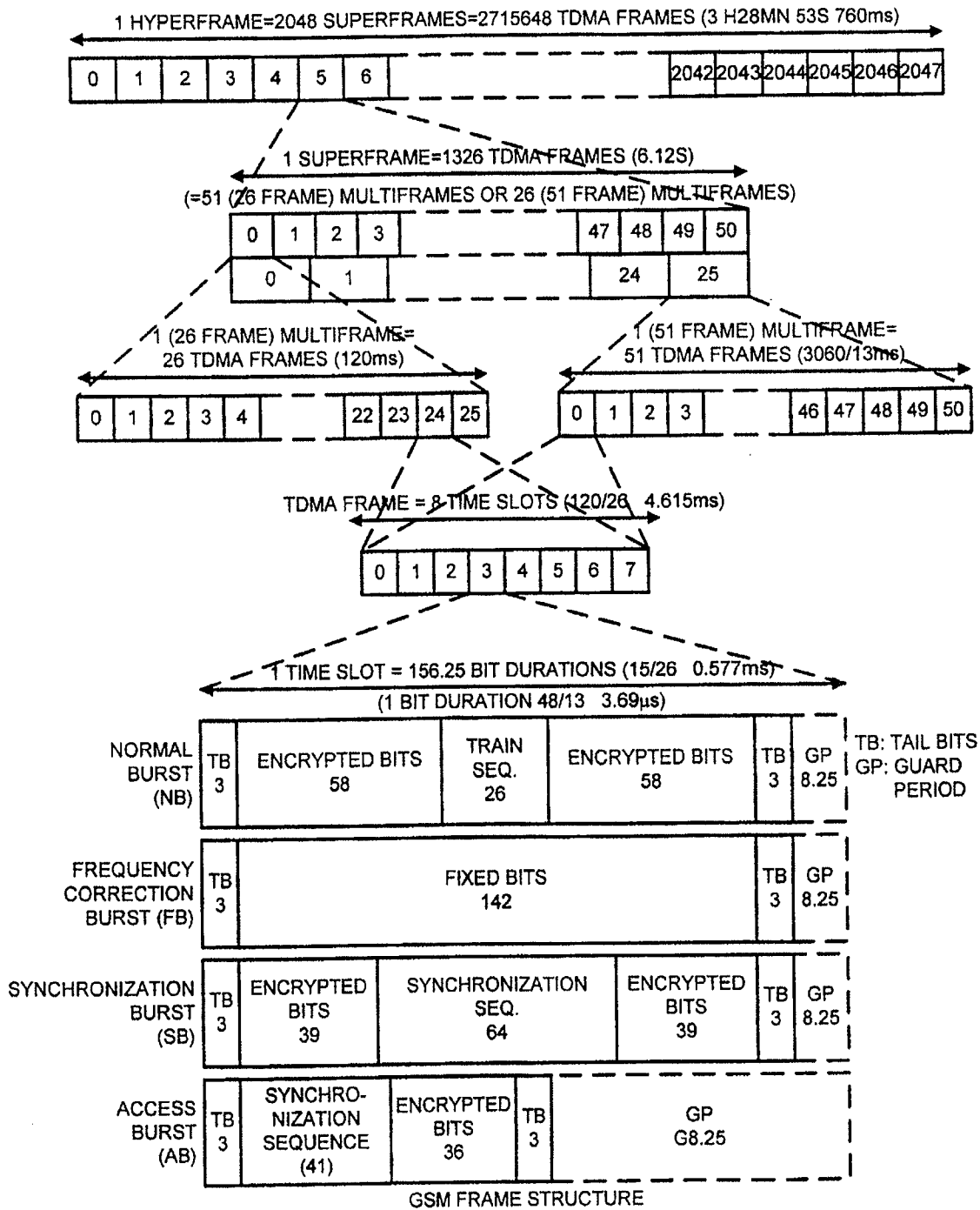


FIG. 1(c)

PRIOR ART

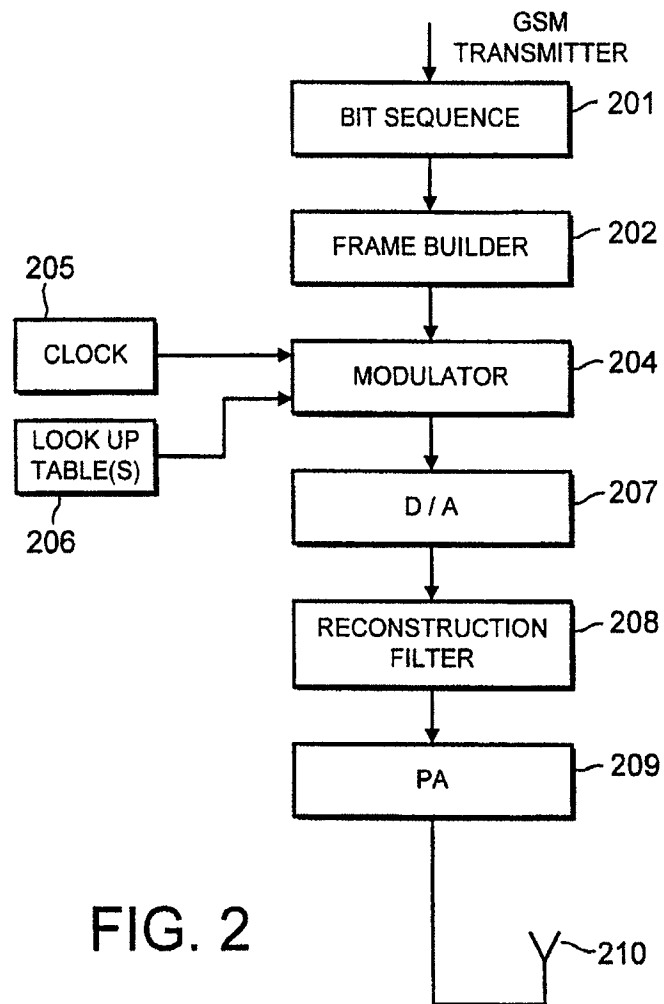


FIG. 2

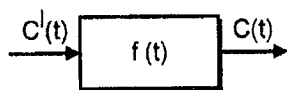
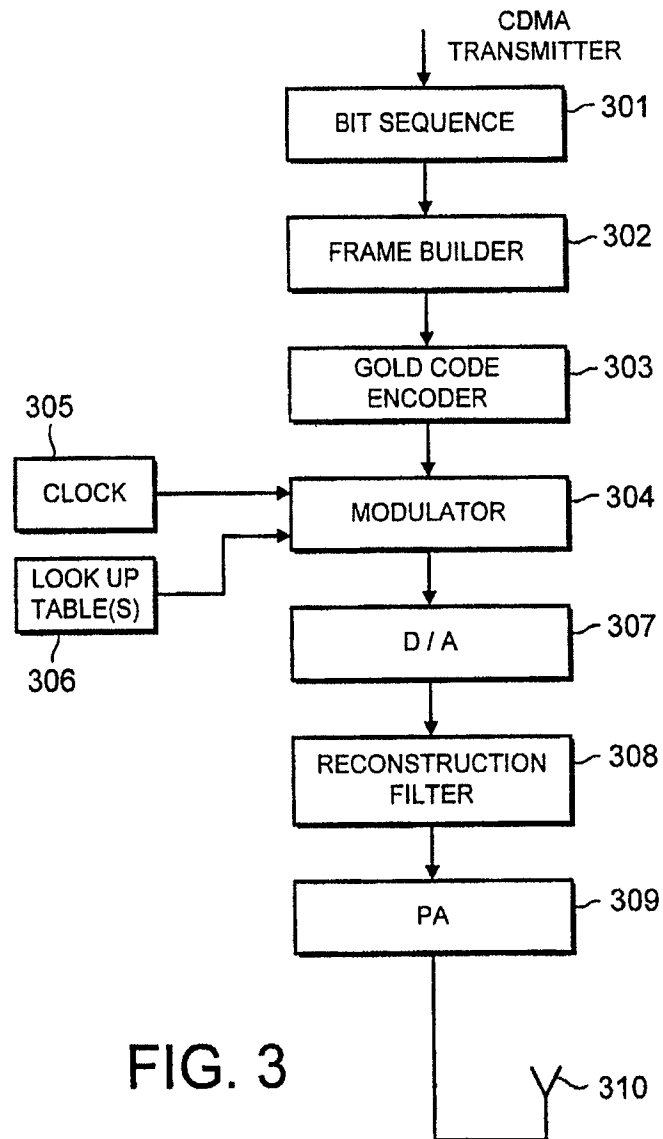


FIG. 4(a)

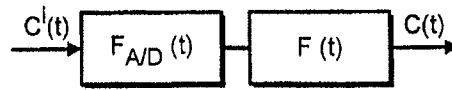


FIG. 4(b)

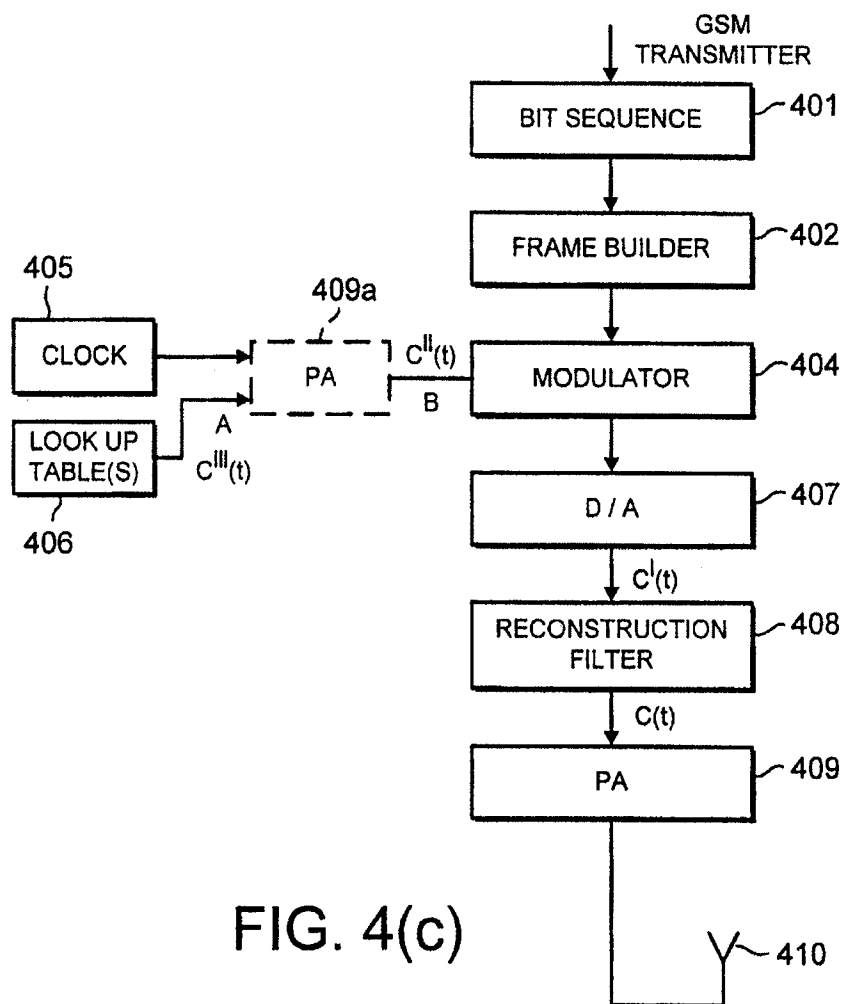


FIG. 4(c)

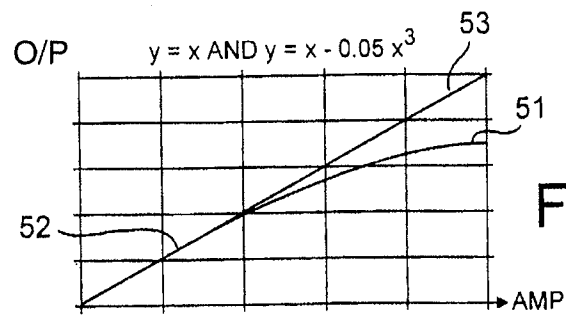


FIG. 5(a)

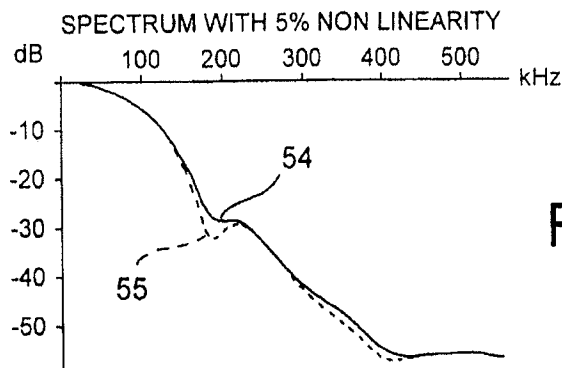


FIG. 5(b)

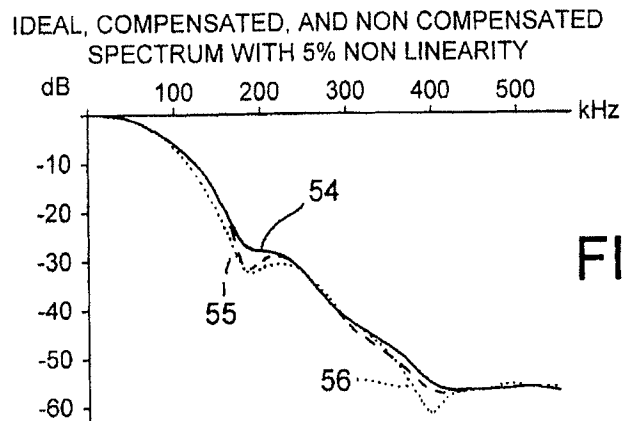


FIG. 5(c)

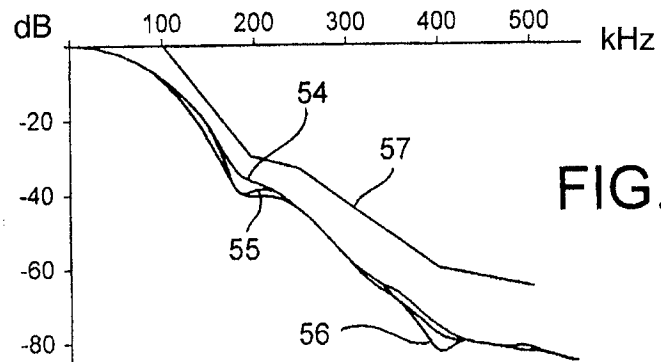
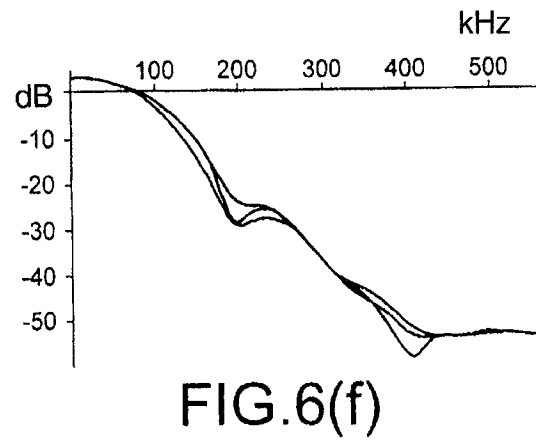
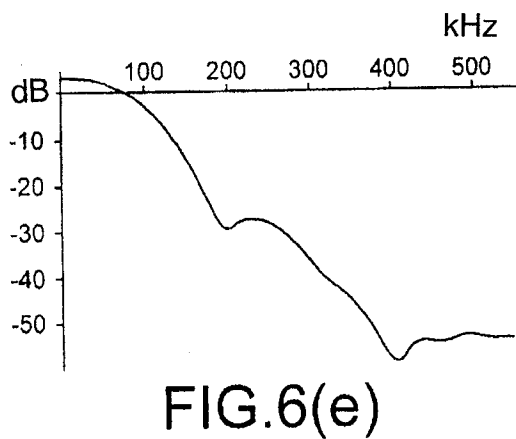
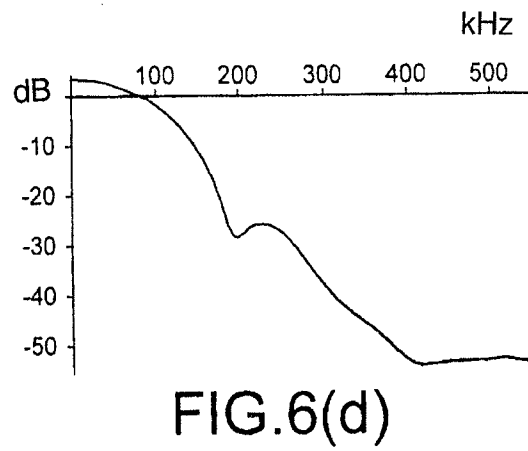
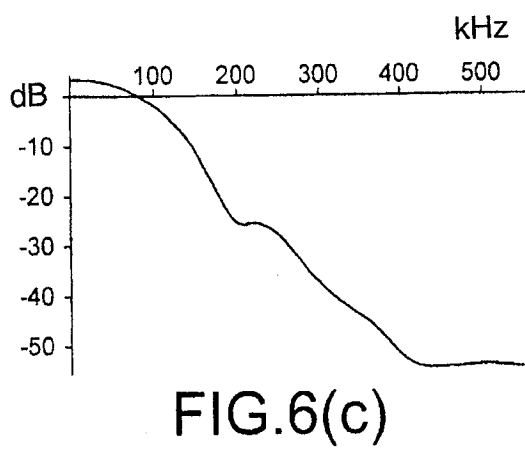
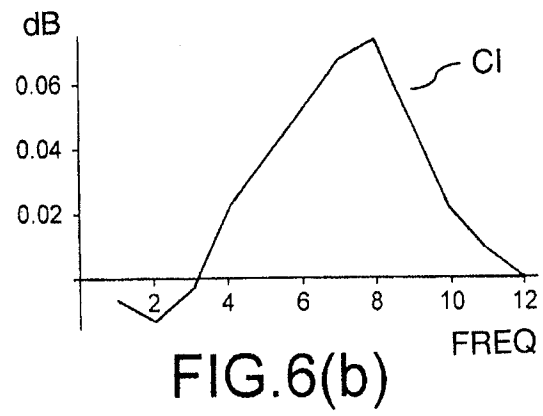
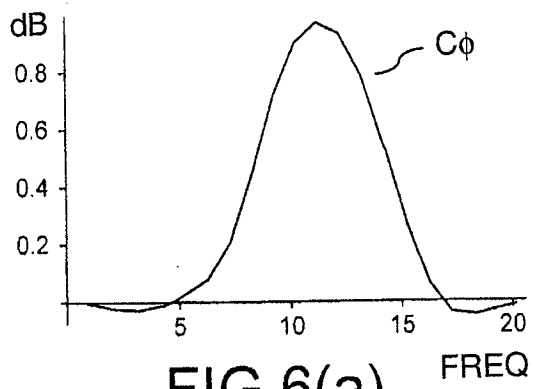


FIG. 5(d)



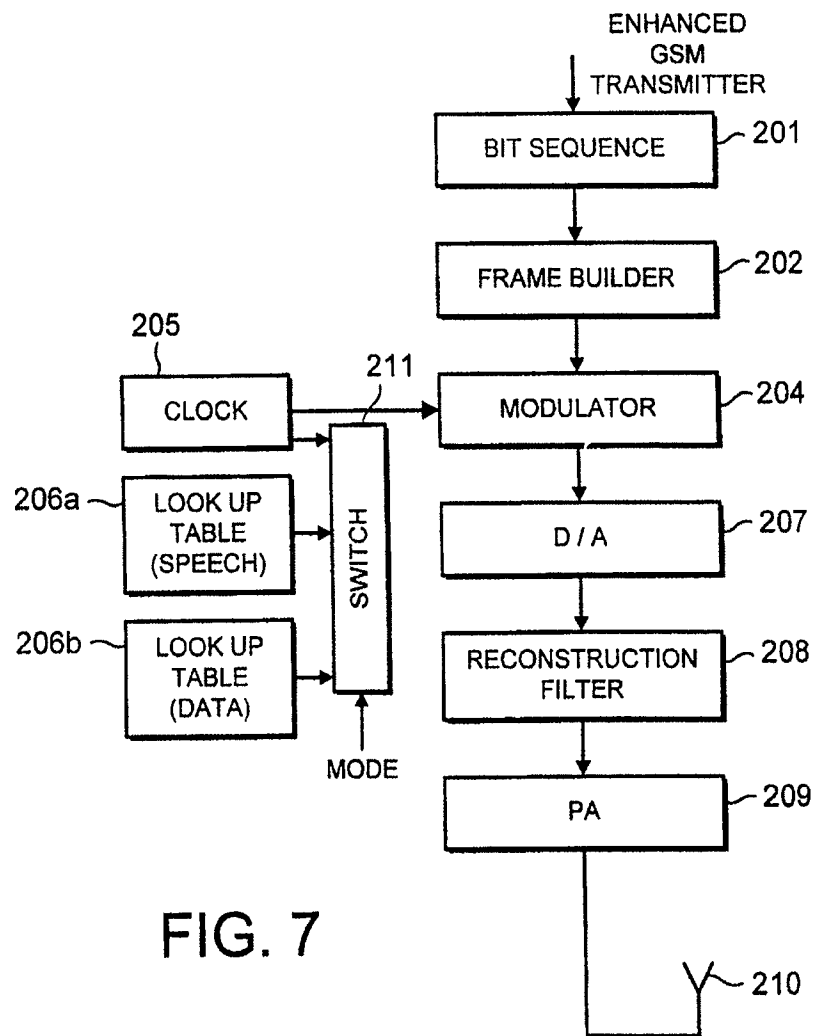
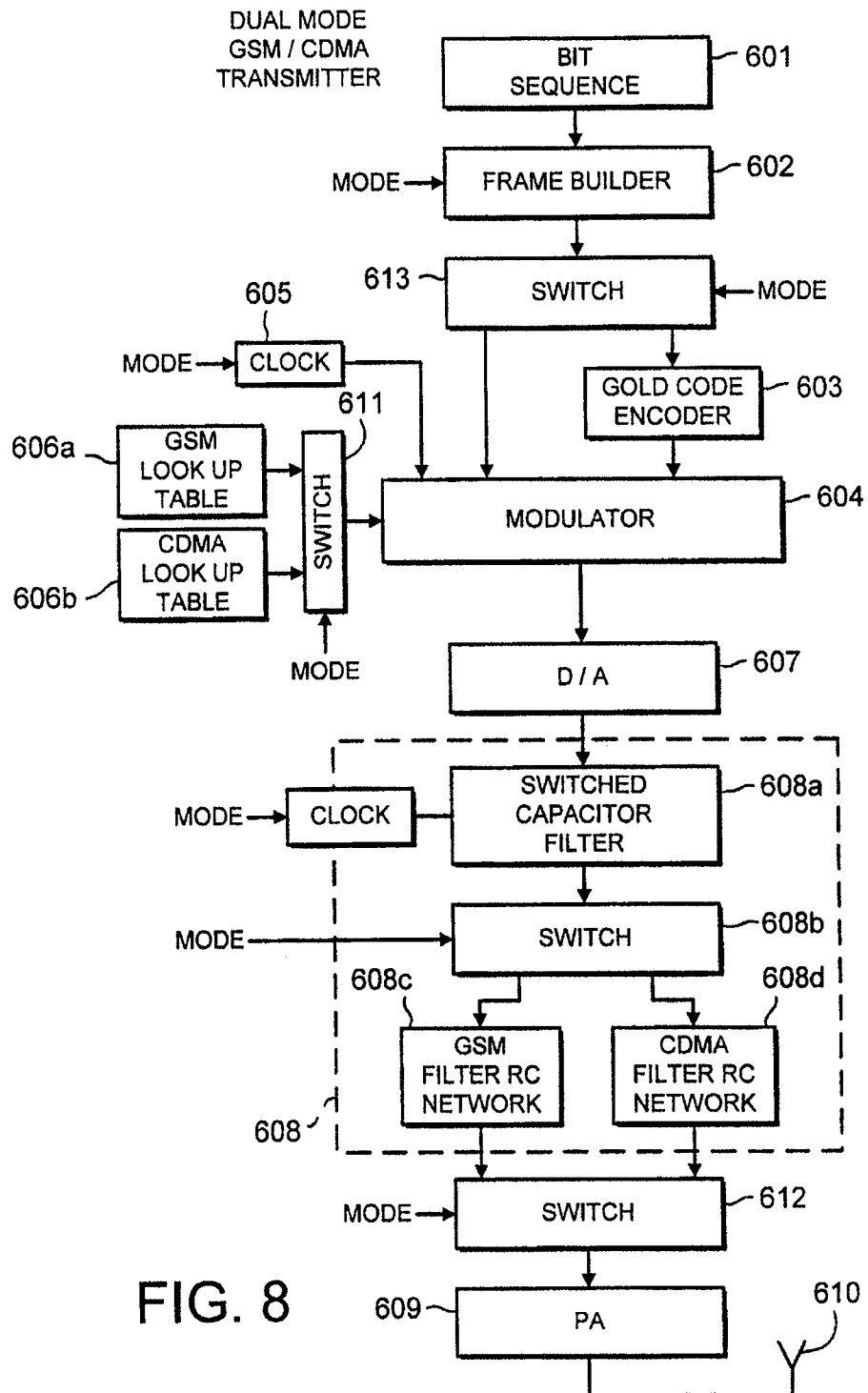


FIG. 7



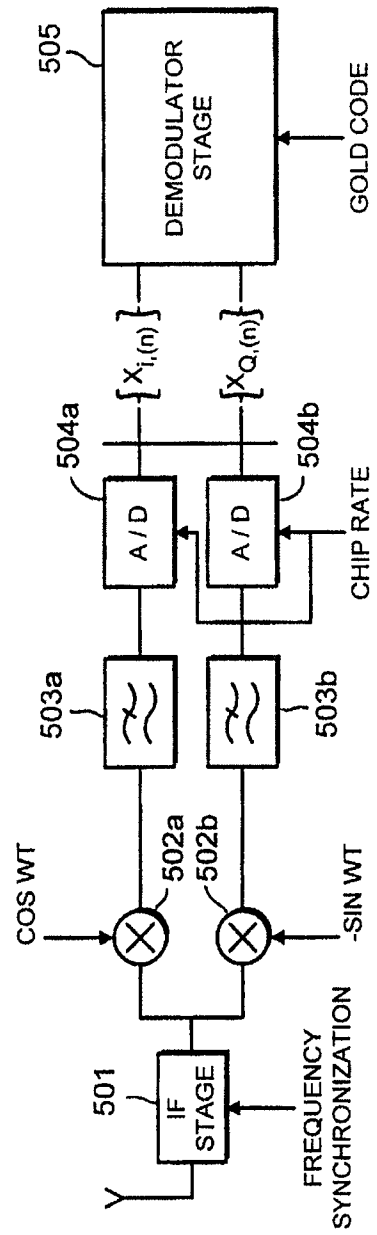


FIG. 9

PRIOR ART

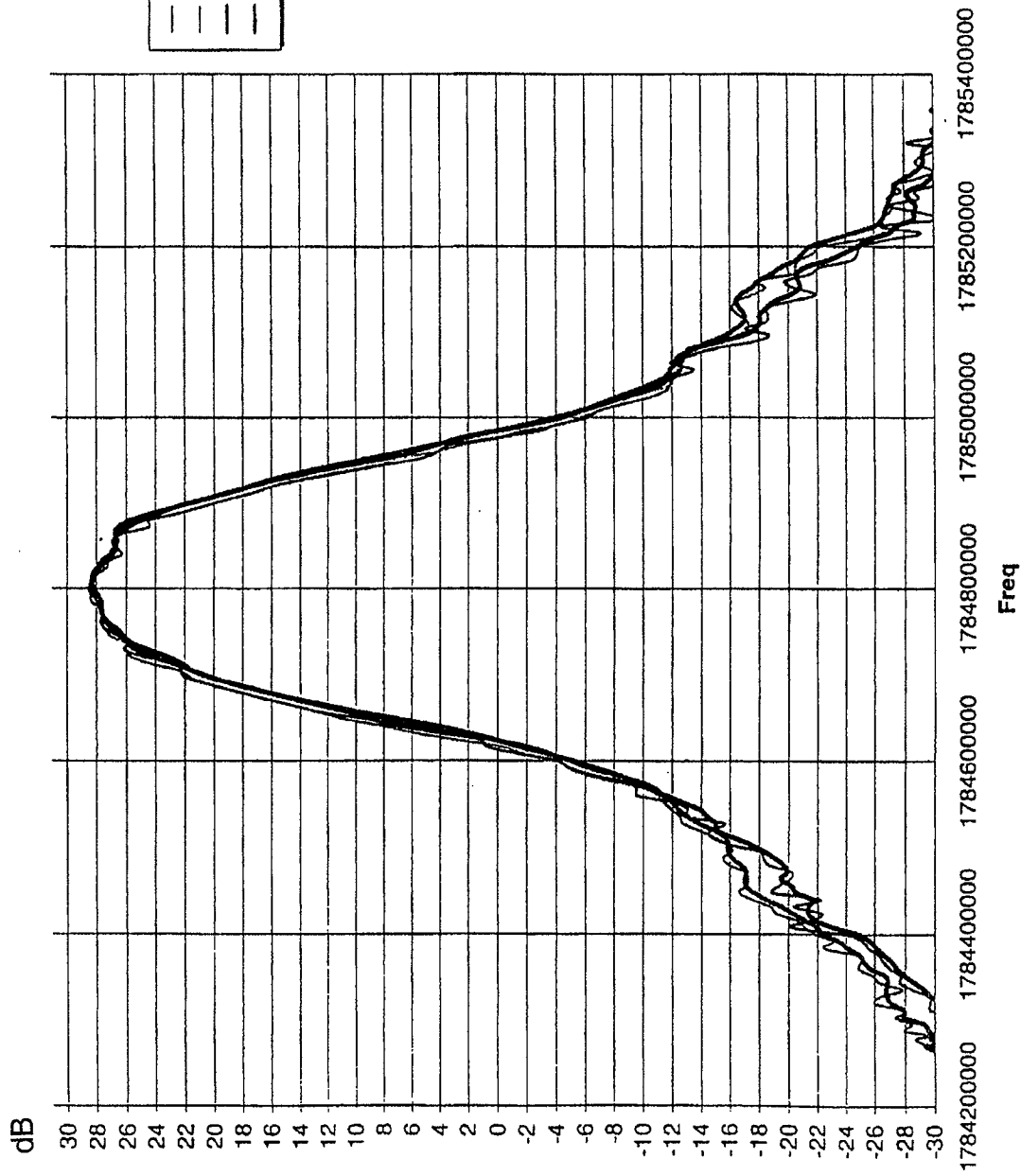


FIG.10(a)

PHASE ERROR rms max

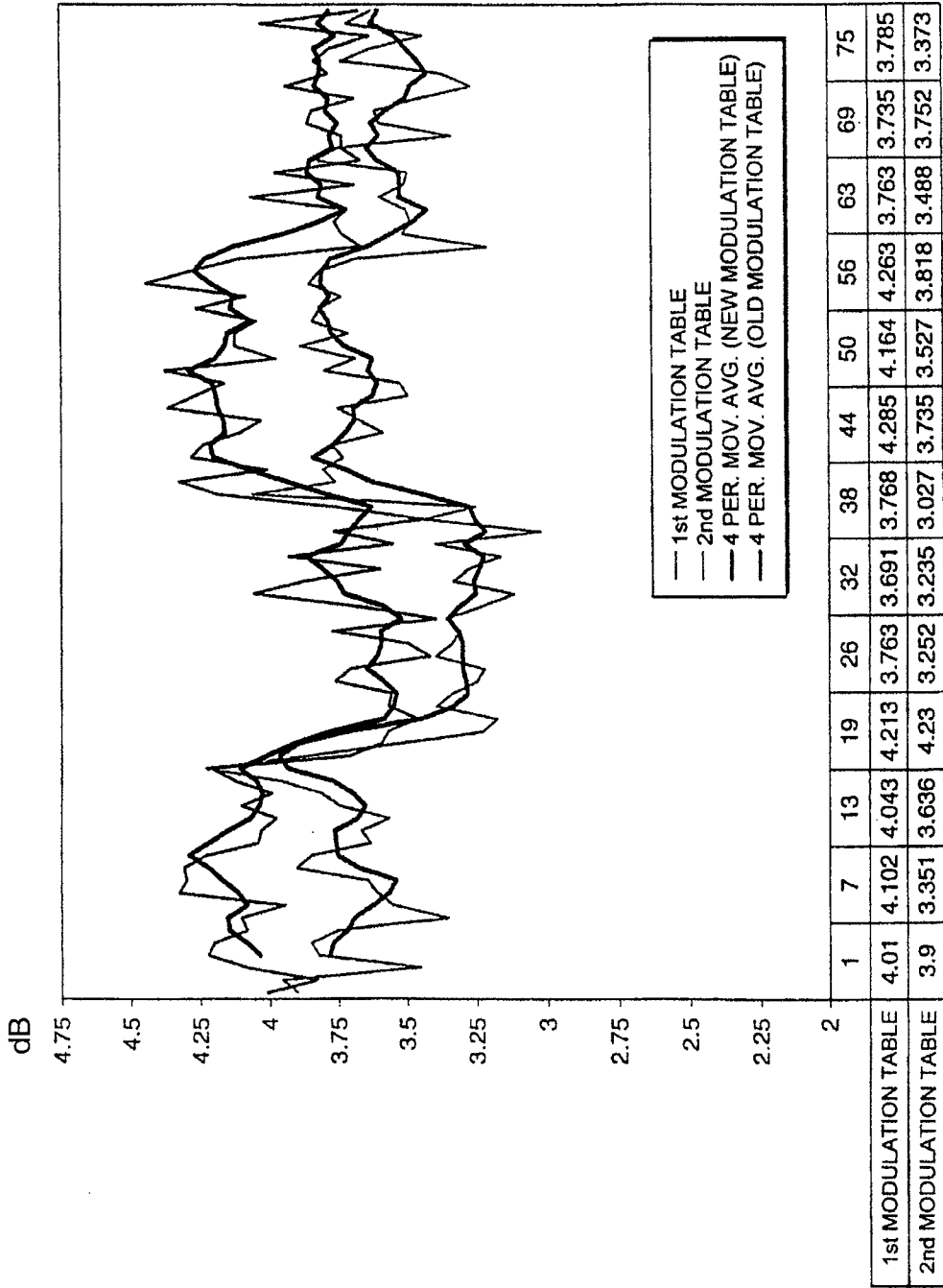


FIG.10(b)

Frequency